APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Paragraph at page 2, line 19:

a1

In circuit 40, power FET 42, for example, represents either FET 12 or FET 14, with its gate connected either to the LO or the HO pin, which in turn receives gate control voltage from driver 44, representing either driver 22 or driver 30 on IC 20. Similarly, comparator 46 represents either comparator 24 or comparator 32, and buffer 48 represents either buffer 26 or buffer 34. Comparator 46 serves as part of sensing circuitry, providing a sense result signal in response to a sense input signal that includes information received at the DS/VF pin. The sense result signal at the output of comparator 46 includes information derived from the sense input signal about operation of FET 42.

Paragraph at page 5, line 17:

a2

A central cause of the sensing problem is diode capacitance coupling during an off-to-on transition, leading to inaccurate VFB signal timing. As a result of coupling across diode 60, negative spikes and other spurious voltage variations can reach the DS/VF pin and cause inaccurately timed state changes by comparator 46. In addition, changes in the sizes of FET 42 and diode 60 as well as changes in the board and in the slope of segment 110 can affect VFB signal timing, contributing to VFB inaccuracies.

Paragraph at page 6, line 3:

a3

Like the circuits described above, the new circuit includes sensing circuitry, which can include a comparator as described above or other appropriate components to provide a sense result signal in response to a sense input signal. The sense input signal includes information received through a gating device, such as a diode or other appropriate device connected between the sensing circuitry and a power device; the sense result signal in turn includes information derived from the sense input signal about operation of the power device.

Paragraph at page 11, line 9:

During the off-to-on transition of FET 42, diode 60 remains temporarily off and therefore acts as a capacitor, so that a high frequency negative spike could pass through to the DS/VF pin. But segment 202 continues at the same voltage because an active impedance, provided either by element 162 in Fig. 4 or transistor 192 in Fig. 5, holds the voltage at the DS/VF pin and sinks high frequency spikes. As a result, the active impedance prevents the spikes from reaching the "+" input of comparator 46, and segment 204 continues at the same voltage because the output from comparator 46 is unchanged.

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CLAIMS (with indication of amended or new):

Sub B2 a5

AMENDED 1. A power control circuit for controlling power provided across a power device by a driving circuit, comprising:

sensing circuitry for providing a sense result signal_for controlling said driving circuit in response to a sense input signal, the sense input signal including information received through a gating device connected between the sensing circuitry and the power device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received from the gating device.

Sub B2 a6

AMENDED 9. An integrated power control circuit for controlling power provided across a power device by a driving circuit, comprising:

a sensing node for connecting to the power device through a gating device;

sensing circuitry for providing a sense result signal for controlling said driving circuit in response to a sense input signal, the sense input signal including information received at the sensing node through the gating device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received at the sensing node from the gating device.

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Sub B2

AMENDED 17. An integrated power control circuit for controlling power by respective high side and low side driving circuits across high and low side power devices connected in a half bridge, the circuit comprising high side circuitry for controlling the high side power device and low side circuitry for controlling the low side power device;

the high side circuitry comprising:

a first sensing node for connecting to the high side power device through a first gating device;

first sensing circuitry for providing a first sense result signal_for controlling said high side driving circuit in response to a first sense input signal, the first sense input signal including information received at the first sensing node through the first gating device; the first sense result signal including information derived from the first sense input signal about operation of the first power device; and

first correction circuitry for preventing the first sense input signal from including spurious information received at the first sensing node from the first gating device; and

the low side circuitry comprising:

a second sensing node for connecting to the low side power device through a second gating device;

second sensing circuitry for providing a second sense result signal for controlling said low side driving circuit in response to a second sense input signal, the second sense input signal including information received at the second sensing node through the second gating device; the second sense result signal including information derived from the second sense input signal about operation of the second power device; and

second correction circuitry for preventing the second sense input signal from including spurious information received at the second sensing node from the second gating device.

Sub B2

a8

NEW 18. The circuit of claim 1, further comprising a driving circuit, wherein a driving circuit, receives an input voltage and generates a driving signal for providing said power across said power device.

NEW 19. The circuit of claim 9, further comprising a driving circuit, wherein said driving circuit receives an input voltage and generates a driving signal for providing said power across said power device.

cont a8

NEW 20. The circuit of claim 17, wherein

said high side circuitry further comprises a high side driving circuit, wherein said high side driving circuit receives an input voltage and generates a driving signal for providing said power across said high side power device; and

said low side circuitry further comprises a low side driving circuit, wherein said low side driving circuit receives an input voltage and generates a driving signal for providing said power across said low side power device.

NEW 21. The circuit of claim 9, in which the gating device provides spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.

NEW 22. The circuit of claim 17, in which the gating device provides spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.